

### **REMARKS**

Claim 17 stands rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement, and second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements. Applicants respectfully traverse the rejections.

The Examiner identifies FIGs. 14-a and 14-c as having the closest structure to that recited in claim 17. This is incorrect. FIG. 25B shows an electrostatic protection element portion having a multi-layered structure metal layer 200d in which a top layer is partially removed and an underlayer directly below the top layer is exposed. An insulating layer 54 is formed on the metal layer. A contact hole 98 is formed by opening the insulating layer 54 on the metal layer. A connecting layer 43 electrically connects the top layer and the underlayer of the metal layer via the contact hole. (See FIG. 25 and related description in Applicants' specification). Thus, in light of this explanation, withdrawal of the §112 rejections of claim 17 is respectfully requested.

Claim 14 stands rejected under 35 U.S.C. 102(b) as being anticipated by Shimada. In response, Applicants amended independent claim 14 to clarify that the insulating layer directly formed on a plurality of metal layers is formed so as to completely cover surfaces of the plurality of metal layers, and respectfully traverse the rejection because Shimada fails to disclose or suggest a connecting layer electrically connecting the metal layers via the contact hole.

As shown in FIG. 6B, Shimada has a gate electrode 11a surrounded by an insulating film 12a, a transparent substrate 112, and a transparent electrode layer 16a. Short resistors 106a are formed adjacent to the gate electrode 11a, and contact the transparent electrode layer 16a. In the Office Action, the Examiner equates the electrostatic protection element portion of the present invention with the short resistors 106a of Shimada. A plurality of metal layers is defined by the Examiner as corresponding to each neighboring terminal pad 107 with an insulating layer 112 formed on the plurality of metal layers. The Examiner further asserts that a contact hole is formed by opening the insulating layer on the plurality of metal layers in the region above gate electrode 11a. However, there is no contact hole formed in the transparent substrate 112. Therefore, the transparent substrate 112 cannot correspond to the insulating layer of the present invention.

Nevertheless, even if another layer could correspond to the insulating layer, Shimada still fails to disclose a connecting layer electrically connecting the metal layers via the contact hole. Gate electrodes 11a are simply not connected to one another by an opening in the contact hole 21, as recited in independent claim 14. For these reasons, withdrawal of the §102(b) rejection of claim 14 is respectfully requested.

Claim 14 stands rejected under 35 U.S.C. 102(b) as being anticipated by Ukai et al. (U.S. Patent No. 5,068,748). Applicants traverse the rejection because the cited reference fails to disclose (or suggest) an insulating layer directly formed on the plurality of metal layers so as to completely cover surfaces of the plurality of metal layers, as now recited in amended claim 14.

Ukai discloses in FIGs. 11A and 11C a semiconductor layer 44 covering a part of a surface of one of the conductor lands 51. An internal short circuiting bus 32 connecting adjacent conductor lands 51 via contact holes 52 is also shown. The internal short circuiting bus 32 is formed on the semiconductor layer 44 and the conductor land 51. However, Ukai fails to disclose or suggest having an insulating layer directly formed on the plurality of metal layers so as to completely cover surfaces of the plurality of metal layers, as now recited in the amended claims. For this reason, withdrawal of the §102(b) rejection of claim 14 is respectfully requested.

Claims 13 and 15 stand rejected under 35 U.S.C. 102(b) as being anticipated by Nakagawa et al. (U.S. Patent No. 5,650,834). Nakagawa merely discloses in FIGs. 7(a) and (b) three layers, which include a Cr film 64, a Al film 65, and a thin film resistor 6 connecting the input terminal 4a to a short ring 7 via the contact holes 61a and 61b. However, Nakagawa fails to disclose or suggest a connecting layer electrically connecting the metal layers via the contact hole. More specifically, the input terminal 4a is not formed of a plurality of metal layers that has one of the layers removed while a connecting film connects the metal layers, as shown in FIG. 25 of the present application. For this reason, withdrawal of the §102(b) rejection of claims 13 and 15 is respectfully requested.

Claims 13 and 15 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Shimada, and further in view of Shiraki et al. (U.S. Patent No. 5,926,234). Applicants respectfully traverse the rejection because the cited references fail to disclose or suggest a connecting layer electrically connecting the metal layers via the contact hole.

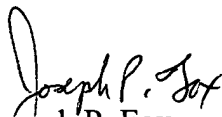
Shimada fails to disclose the connecting layer of the present invention as discussed above. Shiraki is merely cited by the Examiner as disclosing the addition of a ground ring (first and second common lines) and terminals, in addition to elements between the terminals. Accordingly, since the combination of references fails to disclose or suggest a connecting layer electrically connecting the metal layers via a contact hole, withdrawal of the §103(a) rejection of claims 13 and 15 is respectfully requested.

Finally, Applicants have also added new dependent claims 18-20, and respectfully submit that the new claims are allowable for at least the reasons discussed above related to their associated independent claims.

For all of the foregoing reasons, Applicants submit that this Application is in condition for allowance, which is respectfully requested. The Examiner is invited to contact the undersigned attorney if an interview would expedite prosecution.

Respectfully submitted,

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